Epitaxial growth of InP nanowires on germanium

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The growth of III–V semiconductors on silicon would allow the integration of their superior (opto-)electronic properties[1–3] with silicon technology. But fundamental issues such as lattice and thermal expansion mismatch and the formation of antiphase domains have prevented the epitaxial integration of III–V with group IV semiconductors[4–6]. Here we demonstrate the principle of epitaxial growth of III–V nanowires on a group IV substrate. We have grown InP nanowires on germanium substrates by a vapour–liquid–solid[7] method. Although the crystal lattice mismatch is large (3.7%), the as-grown wires are monocrystalline and virtually free of dislocations. X-ray diffraction unambiguously demonstrates the heteroepitaxial growth of the nanowires. In addition, we show that a low-resistance electrical contact can be obtained between the wires and the substrate.

With the development of the vapour–liquid–solid (VLS) method[7] for wire growth it has become possible to grow nanowires with built-in heterojunctions[8–10]. The formation of an almost atomically sharp heterojunction has been demonstrated in an InAs/InP nanowire[8]. For these wires it was suggested that the mechanical stress induced by the lattice mismatch (3.1%) is relieved laterally at the wire surface, and this idea is supported by a detailed analysis of the electrical characteristics[11]. Homoepitaxial growth of nanowires on bulk substrates has been proposed for several semiconductor systems such as germanium[12], silicon[13], InAs and GaAs (ref. 14), and heteroepitaxial growth has been suggested for germanium wires on silicon[15] and GaN (ref. 16) and ZnO (ref. 17) on sapphire substrates. In these systems, the nanowires are geometrically oriented, which gives an indication of epitaxial growth. Crystallographic evidence for epitaxial wire growth has not, however, been presented so far. Moreover, heteroepitaxial growth of III–V nanowires on a group IV semiconductor has not been addressed at all.

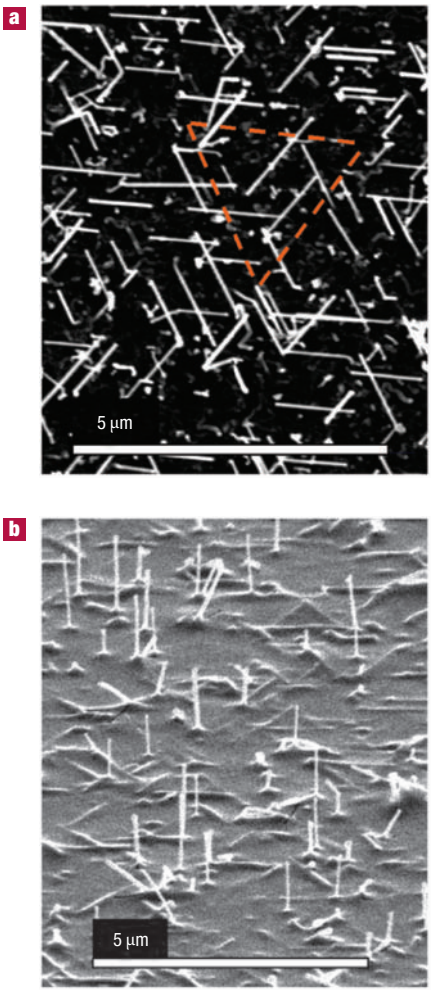

Figure 1 Scanning electron microscopy images of two samples with InP nanowires grown on Ge(111). a, Top-view image showing wires aligned according to the crystal symmetry of the substrate. **b**, Side-view image after spin-coating of a PMMA layer.

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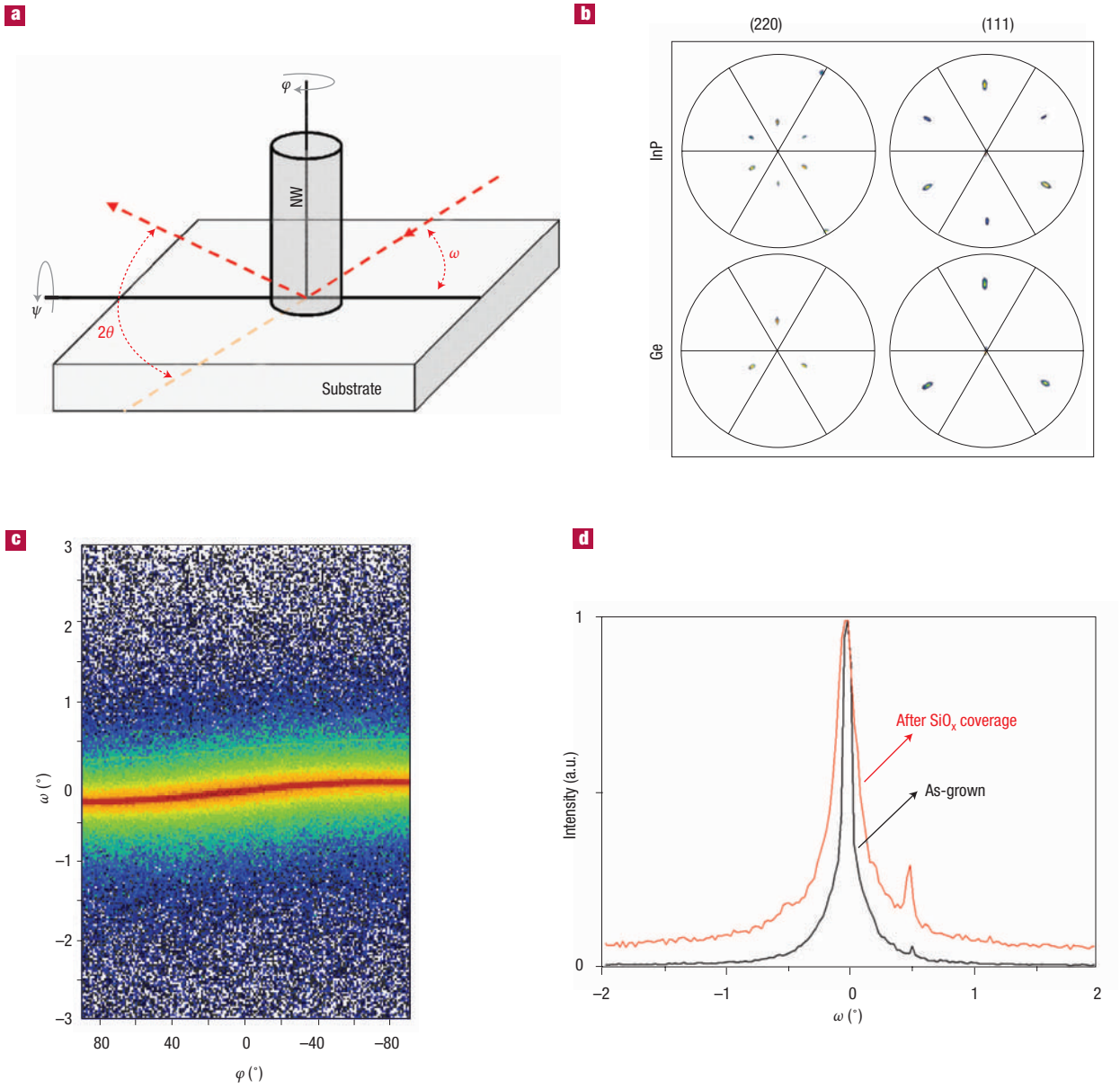

Figure 2 The crystallographic relation between the InP wires and the Ge substrate studied by X-ray diffraction. a, Illustration of the experimental geometry. NW indicates the nanowire. **b**, X-ray diffraction pole figures for the (111) and (220) reflections from the InP nanowires and the Ge(111) substrate. To record the pole figure, the detector was set at a 2θ angle corresponding to one of these reflections and the substrate was rotated continuously around φ (see Fig. 2a), and stepped around ψ ($\Delta\psi = 2°$). **c**, High-resolution pole figure on colour scale (intensity increases from blue to green, yellow and red) of the (111) InP planes parallel to the Ge surface. A scan in the ω direction (with a resolution of 0.005°) was recorded at different φ rotation angles (φ was varied in steps of 1°). The small curvature in the maximum is due to a small physical misalignment of the sample. **d**, Normalized rocking curves (ω scans), extracted from the high-resolution pole figure, of an as-grown sample (black) and of a sample covered with PECVD SiO_x (red). The full-width at half-maximum (FWHM) of the peak corresponds to 0.09° for an as-grown sample and to 0.25° after the wires were embedded in SiO_x. The small signal at $\omega = 0.5°$ is a detector artefact.

Here we demonstrate the viability of integrating III–V nanowires structurally and electrically with a group IV substrate. For this study, InP nanowires were grown on Ge(111), which corresponds to the preferential growth direction for these nanowires, and on Ge(100) substrates, which relates to the standard orientation for silicon technology. Germanium was chosen (instead of the more frequently used silicon) because of the less troublesome procedure for removing the surface oxide.

The substrates were cleaned in a buffered HF etch and were provided with the equivalent of a 2-Å gold film by thermal evaporation. On heating, the gold film breaks up into small particles from which the nanowires grow by the VLS method[7]. The substrate temperature during synthesis was 430–490 °C, as reported previously[18].

A top-view scanning electron microscopy (SEM) image of a Ge(111) substrate with as-grown InP wires is shown in Fig. 1a.

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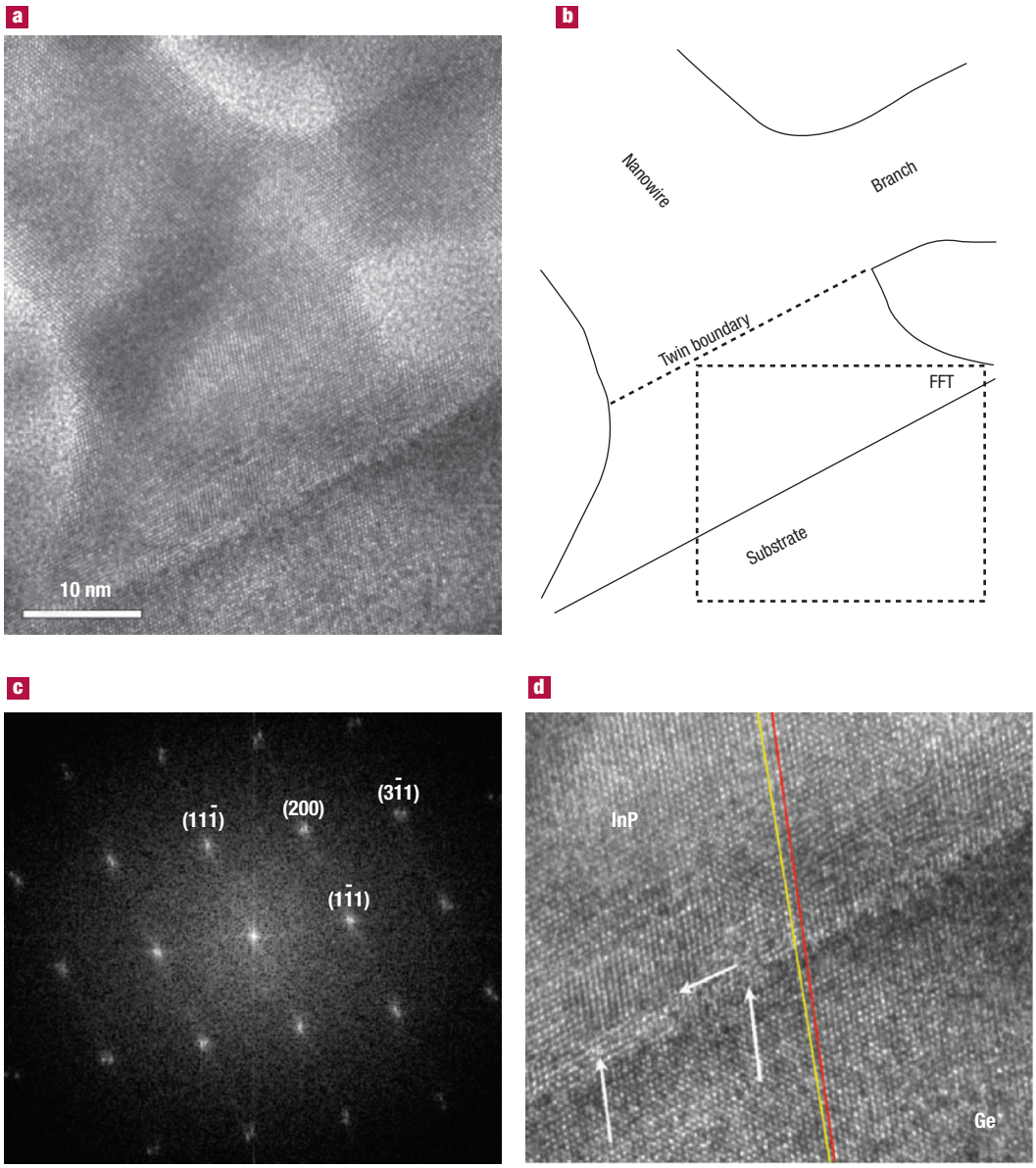

Figure 3 TEM images of an InP wire on a germanium substrate. a, High-resolution TEM image of an InP wire on a Ge(111) substrate. The dark spots are amorphous deposits resulting from the focused-ion-beam treatment. **b**, Contour drawing of the sample elucidating the geometry in **a**. **c**, Fast Fourier transformation (FFT) calculated for the rectangular field delimited by a dashed line in **b**. The double spots in the FFT pattern correspond to the InP and Ge reciprocal lattices. **d**, The interfacial area between the InP wire and the Ge crystal. The arrows indicate the locations of three misfit dislocations. The lines parallel to the $(1\bar{1}1)$ lattice planes of the substrate (red) and the wire (yellow) illustrate the anticlockwise lattice tilt of the wires.

The wires have a uniform diameter and a length of ~1 μm. There are three clearly noticeable orientations with in-plane components parallel to the sides of an equilateral triangle, which is drawn as a guide to the eye. Some wires are oriented perpendicular to the surface, and in this top view they appear just as small bright spots. The observed preferential orientations correspond to the four ⟨111⟩ directions typical for a (111) oriented crystal; one orientation perpendicular to the surface and three orientations forming a 19° angle with the surface and having in-plane components at 120° from each other. The fact that nanowires have well-defined orientations consistent with the substrate's crystal symmetry is a clear indication of epitaxial growth. To substantiate this claim further we have made X-ray diffraction (XRD) and transmission electron microscopy (TEM) measurements.

The crystallographic relation between the Ge substrate and (a large number of) InP nanowires was studied by XRD pole figure measurements. Pole figures were measured for the (111) and (220) reflections as explained in Fig. 2a. The pole pattern (Fig. 2b) associated with the majority of the wires (that is, about two-thirds of the total signal) matches the pole pattern of the substrate, providing an unambiguous signature of heteroepitaxial growth. The rest of the wires show a 180° in-plane rotation with respect to the Ge crystal, which we ascribe to twinning defects at the Ge/InP interface or inside the wires. The fact that the mirrored orientations give a lower signal

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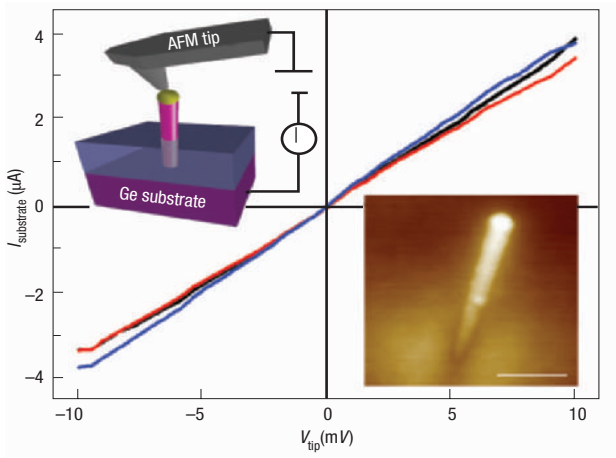

Figure 4 Transport measurements through an epitaxially grown nanowire by means of an AFM. Current–voltage curves of a single n-type InP nanowire grown on n-type Ge(111). The three traces were taken on the same wire after lifting and repositioning the conducting AFM tip on the catalytic particle. Inset (top): Schematics of the measurement configuration. Inset (bottom): AFM image of an InP nanowire grown on n-type Ge(111). The scale bar corresponds to 250 nm.

than the orientation identical to the substrate reveals that the density of twinning defects is low. Most probably a large fraction (half) of the wires was grown without twinning defects at all. In the case of InP wires grown on Ge(100) substrates, also, XRD pole figures illustrate that wire growth is epitaxial (see Supplementary Information).

The possible existence of a tilt in the crystal structure of the nanowires with respect to the substrate was studied in more detail by means of high-resolution pole measurements (Fig. 2c). These measurements demonstrate that the crystal lattice orientation of the wires is identical (±0.09°, see Fig. 2d) to that of the substrate. In particular, we have not observed reflections at $\omega = \pm 1.4°$ from the main peak (at every $\Delta\varphi = 120°$), which would be expected if a fraction of the wires had Shockley partial dislocations (SPDs; see TEM results below).

The wire–substrate interface of individual wires was investigated by TEM. For this study, a vertical cross-section was sliced and thinned with a focused ion beam (FIB). To provide mechanical support during this process, the wires were embedded in a 2-μm-thick SiO_x layer, deposited by spin-on process or by plasma-enhanced chemical vapour deposition (PECVD). Figure 3a shows a cross-sectional high-resolution TEM image taken at the base of an InP wire; the epitaxial relation between the nanowire and the substrate is apparent from this image. The wire has a uniform diameter of 21 nm with a significant broadening at the base. The tapering of the base of the wire is a result of the fact that a concave region (wire–surface interface) will grow faster than a flat crystal face in order to reduce the surface energy. At 15 nm from the substrate surface a second (thinner) wire intersects the vertical wire (illustrated in Fig. 3b), causing a rotational twin dislocation; no more dislocations can be found further up. Similar inspections on four other wires also showed the epitaxial relation between the wire and the substrate, but did not show such accidental branching. In all these cases, however, the wire–substrate interface is less clear owing to poor transparency of the slice or to the damage caused by FIB milling. A fast Fourier transformation (FFT) of the TEM image was taken on a 25×25 nm^2 rectangular field across the InP/Ge interface (see Fig. 3b). Double spots were observed (Fig. 3c) corresponding to the InP and Ge reciprocal lattices along the [011] zone axis. The lattice spacings corresponding to the InP wire, as extracted from the FFT pattern, are 0.5% lower than the literature values[19] for InP. This shows that for this wire the InP lattice is almost, but not fully, relaxed within a few nanometres from the Ge substrate. (High-resolution XRD measurements revealed that the crystal lattice parameters of the bulk of the wires correspond to the literature values.)

Additionally, the angle between equivalent spots of Ge and InP was studied. This shows that the InP lattice is rotated $1.4 \pm 0.3°$ around the [011] zone axis with respect to the Ge lattice. A similar lattice tilt angle was observed in the four other wires studied by high-resolution TEM. In Fig. 3d the interfacial area is shown in detail. The arrows point to the position of three misfit dislocations, one parallel to the surface, and two parallel to the $(1\bar{1}1)$ planes. The parallel dislocation, which is a result of an inserted lattice plane parallel to the substrate surface, leads to the anticlockwise tilt of the wire crystal lattice with respect to that of the substrate. This combination of SPDs has been indicated as a mechanism to accommodate strain in Si–Ge systems[20].

The presence of SPDs (and the resulting lattice tilt) in all the wires studied by TEM contrasts with the previously discussed XRD results for the as-grown samples, where no traces of such dislocations were found. To investigate the role of sample processing we compared XRD measurements done before and after SiO_x deposition. No relevant changes were found in the pole figures, except for a broadening of the peaks in the high-resolution pole measurements, which could be ascribed to a small fraction of bent wires (Fig. 2d). Because no evidence of a tilt was found in the XRD experiments, we conclude that SPDs were induced during the FIB process. The atomic layers closest to the heterointerface of the as-grown nanowires are under compressive strain, which can relax during sample preparation through the introduction of SPDs.

The structural studies presented so far demonstrate that crystalline InP nanowires can be epitaxially grown on a Ge substrate, despite the substantial lattice mismatch. The next step is to prove that the heterointerface can form a good (low-resistance) electrical connection between the wire and the substrate. This is the premise for an efficient electrical integration between III–V vertical devices (light-emitting diodes, lasers or gate-around transistors[21]) with the group IV substrate. To address this important issue, we used Se-doped n-type InP nanowires on n-type Ge(111). The wires were partially embedded in an insulating poly(methylmethacrylate) (PMMA) layer deposited by spin-coating (1000 r.p.m.) and annealed at 175 °C. Figure 1b shows an SEM image of a sample provided with a 100-nm PMMA layer. Evidently, many wires protrude from the PMMA layer and have preserved their orientation even after the spin-coating process.

Electrical transport measurements through individual wires were made in an atomic force microscopy (AFM) set-up. A platinum-coated AFM tip was scanned in contact mode over the surface, while a tuneable d.c. voltage was simultaneously applied between the tip and the back of the Ge substrate (Fig. 4a). A non-zero current through the substrate was measured when an electrical contact was established between the tip and the catalytic metal particle at the top of a nanowire. Because of PMMA residues, the resistance varied from place to place on the catalyst particle. Current–voltage characteristics of tens of individual wires were measured, yielding resistance values down to a few kilo ohms (Fig. 4b). This value represents an upper limit for the wire–substrate interface resistance, which corresponds to a very low contact resistivity of less than $\sim 10^{-8}\ \Omega\ \mathrm{cm}^2$. This low-resistance ohmic behaviour can be explained by the relatively small (~40 meV) conduction-band offset between Ge and InP (ref. 22) and by the deliberately high doping levels (10^{18}–10^{19} cm^{-3}) in both the InP wires and the Ge substrate. Because Ge is preferentially an n-type dopant for InP (ref. 23,24) we expect that a very good

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electrical contact can also be achieved with moderately doped InP wires by means of interdiffusion.

The current progress in growing strain-relaxed germanium layers on silicon wafers[25] implies that III–V semiconductor nanowires can be combined structurally and electrically with silicon technology. This represents an important step towards the final goal of bringing new materials and hence new device architectures into silicon-based integrated circuits. However, the most desirable goal of epitaxially growing III–V nanowires directly on silicon remains unattained. Besides the problem of a suitable procedure for oxide-free surface preparation, the limits to the lattice mismatch for heteroepitaxial nanowire growth should be explored (for example, the lattice parameter of InP is 8.7% larger than that of Si). The VLS growth of ternary compound semiconductor nanowires[26] may be a way to engineer the lattice parameter and overcome possible limitations coming from an exceedingly high lattice mismatch. From the results of this work, and the versatility of the VLS method, we believe that the growth of III-V semiconductor wires directly on silicon is now a step closer.

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Competing financial interests

The authors declare that they have no competing financial interests.

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