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Abstract

We report the growth and characterization of InAs nanowires capped with a 0.5–1 nm epitaxial InP shell. The low-temperature field-effect mobility is increased by a factor 2–5 compared to bare InAs nanowires. We extract the highest low-temperature peak electron mobilities obtained for nanowires to this date, exceeding 20 000 cm^2 V s^{-1}. The electron density in the nanowires, determined at zero gate voltage, is reduced by an order of magnitude compared to uncapped InAs nanowires. For smaller diameter nanowires we find an increase in electron density, which can be related to the presence of an accumulation layer at the InAs/InP interface. However, compared to the surface accumulation layer in uncapped InAs, this electron density is much reduced. We suggest that the increase in the observed field-effect mobility can be attributed to an increase of conduction through the inner part of the nanowire and a reduction of the contribution of electrons from the low-mobility accumulation layer. Furthermore the shell around the InAs reduces the surface roughness scattering and ionized impurity scattering in the nanowire.

(Some figures in this article are in colour only in the electronic version)

Nanometer-sized quasi one-dimensional systems, such as semiconducting nanowires (NWs), are attractive building blocks for bottom-up nanotechnology including opto-electronics [1, 2] and manipulation of isolated electron spins [3–5].

Nanowire heterojunctions, both longitudinal [6] and radial [7–9], can be grown defect-free due to the small nanowire radius, which allows strain from lattice mismatch to be relaxed radially outwards. This property allowed epitaxial growth of group III–V on group IV elements in nanowires [10, 11]. InAs is an attractive material because its small bandgap results in a low effective electron mass, giving rise to high bulk electron mobilities (at room temperature 22 700 cm^2 V s^{-1} [12] and at low temperature in planar structures over 600 000 cm^2 V s^{-1} [13]).

For bulk InAs, it is well known that the surface contains a large number of states that lie above the conduction band minimum and can contribute electrons to form a surface accumulation layer with a typical downward band bending between 0 and 0.26 eV [14]. Because of the large surface charge density, the Fermi level for InAs is pinned in the conduction band, which makes it easy to fabricate ohmic contacts without a Schottky barrier. This InAs contact property enabled the observation of the superconductivity proximity effect in nanowires [15]. A surface accumulation layer combined with the large surface-to-volume ratio for InAs nanowires could promise good sensitivity for InAs nanowire sensor applications.

As a fraction of the surface states contributes electrons to the accumulation layer, the InAs surface contains a large number of ionized impurities. Electrons in the accumulation layer therefore experience a much stronger ionized impurity scattering than electrons in the inner InAs region. Furthermore, because of the proximity to the surface,

surface roughness scattering is also strong. This means that electrons in the surface layer have a strongly reduced mobility compared to electrons in the inner material, typically $\mu_{\text{surface}} \sim 4000\ \text{cm}^2\ \text{V}\ \text{s}^{-1}$ [12, 14].

For microns thick planar structures of InAs, conduction is dominated by the electrons flowing through the inner region and mobilities are high. The electron mobility is strongly reduced for sub-micron-sized InAs structures [12, 14], because of the higher surface-to-bulk ratio. At the same time, the total electron density increases for smaller thicknesses.

Indications of a surface accumulation layer in InAs nanowires have been observed in [16], where smaller nanowire diameters show an increase in the total electron density, consistent with the observations on accumulation layers in bulk InAs [12]. For InN nanowires, magneto-resistance measurements showed Altshuler–Aronov–Spivak (AAS) oscillations, suggestive of shell-like conduction through nanowires [17]. Conduction through InAs nanowires with typical diameters under 200 nm can be expected to be strongly influenced by the presence of a surface accumulation layer. The strong ionized impurity and surface roughness scattering in the surface accumulation layer could explain why InAs nanowires typically have low-temperature mobilities of 1000–4000 $\text{cm}^2\ \text{V}\ \text{s}^{-1}$ [15, 18–20]. There have been two reports of InAs nanowires yielding mobilities exceeding $16\,000\ \text{cm}^2\ \text{V}\ \text{s}^{-1}$ [21, 22], although it is not clear what was the reason for the apparent increase compared to earlier reports.

The surface-band bending that causes the accumulation layer for InAs is a crystal surface property; however, the strength of the accumulation is known to be dependent on the surface orientation and termination [14]. Reducing the depth of the band bending will result in a higher relative contribution from the inner electrons to the total conduction and an increase in electron mobility. An alternative approach to increase electron mobility would be to reduce the scattering in the surface channel by reducing the surface roughness and the scattering on surface states by surface passivation. Natural III–V oxides are soft, hygroscopic, compositionally and structurally inhomogeneous [23]. In order to get reproducible electronic properties the oxide needs to be removed and a more stable passivation layer needs to be found. In fact Hang *et al* reported that passivating 20 nm InAs nanowires with 1-octadecathiol molecules shows a room temperature increase in mobilities by almost a factor of 2. They claim that their mobility improvement is due to a reduction of scattering from surface states [20]. Sulphur passivation by ammonium sulfide, $(NH_4)S_x$, removes oxides and prevents nanowire contact areas from oxidation [24]. Sulphur passivated nanowires, however, have stronger band bending at the surface compared to the oxidized nanowires [25]. Therefore, when the entire nanowire is treated, ionized impurity scattering at the surface is expected to increase, effectively lowering the electron mobility.

In this paper, we demonstrate InAs surface passivation by the growth of a 0.5–1 nm epitaxial shell of InP around the InAs nanowire. The InAs/InP interface is virtually without any defects despite the large lattice mismatch. We have extracted the electron mobility from the gate dependence of the current using a simulated nanowire capacitance to the gate. Low-temperature mobility has increased by a factor of 2–5 compared to bare InAs nanowires, in agreement with what Jiang *et al* [9] proposed for a similar system. We also report the highest low-temperature peak electron mobilities reported to this date, exceeding $25\,000\ \text{cm}^2\ \text{V}\ \text{s}^{-1}$. The electron density in the nanowires, determined at zero gate voltage, is reduced by an order of magnitude compared to InAs nanowires. The dependence of density on diameter suggests the presence of an accumulation layer with a reduced electron density at the InAs/InP interface. We suggest that the increase in field-effect mobility can be attributed to an increase of conduction through the inner regions of the nanowire and a reduction of both the surface roughness scattering and the ionized impurity scattering in the accumulation layer.

InAs NWs are grown by metal organic vapor phase epitaxy (MOVPE) via the vapor–liquid–solid (VLS) process [26]. Gold catalyst particles with 5 to 20 nm diameter are randomly dispersed on an InP(1 1 1) substrate. Trimethylindium (TMIn) and arsine (AsH_3) precursors in gas phase are supplied to the InP substrate in the growth chamber. The gases dissolve into the gold particles forming an eutect just below the melting point of InAs. Supersaturation of the gases in the Au particle drives the deposition of crystalline InAs directly under the gold particle pushing the particle upwards. The resulting nanowires have a Wurtzite crystal structure and can be as long as 20 μm. Typically they have diameters of 20–300 nm, see figure 1(*a*). Due to parasitic radial growth the wires are tapered.

In order to investigate the role of surface roughness scattering, a thin layer of InP has been grown around the InAs nanowires to passivate the surface. The offset between the InAs and InP conduction bands of ~0.52 eV gives a strong confinement for the InAs electrons, see inset figure 1(*a*). Moreover, the growth of InP is done in the same MOVPE chamber, which prevents InAs from oxidizing and results in a clean epitaxial interface.

For the InP shell growth, a higher growth temperature is used to make the competing bulk semiconductor growth dominating over the InP VLS growth, resulting in lateral growth of InP around the InAs nanowire. In contrast to earlier InAs/InP wire growth [8] no dopant materials are supplied to the system. The lattice mismatch of 3.1% limits the thickness of InP that can be grown defect-free around the InAs. For bulk materials, the critical thickness for planar junctions between InAs and InP has been calculated and measured to be 2–3 nm [28–30]. The critical thickness for a radial nanowire junction, however, is not known. Due to their circular size and small base, the nanowire critical thickness is expected to be larger than that for planar junctions. It has been observed that 7 to 10 nm InP shells grown around InAs cores show no signs of dislocations due to lattice mismatch [8]. Figure 1(*a*) shows a high-angle annular diffraction (HAADF) TEM cross-section of an InAs nanowire with an InP shell of 7–10 nm. No stacking faults or defects due to the lattice mismatch are visible. However, to avoid strain in the nanowires, we have focused on wires with a thin shell of 0.5–1 nm as estimated from energy dispersive x-ray spectroscopy (EDX) and TEM analysis. The sharpness of the InAs/InP interface is beyond the resolution of the EDX analysis; however, it has been

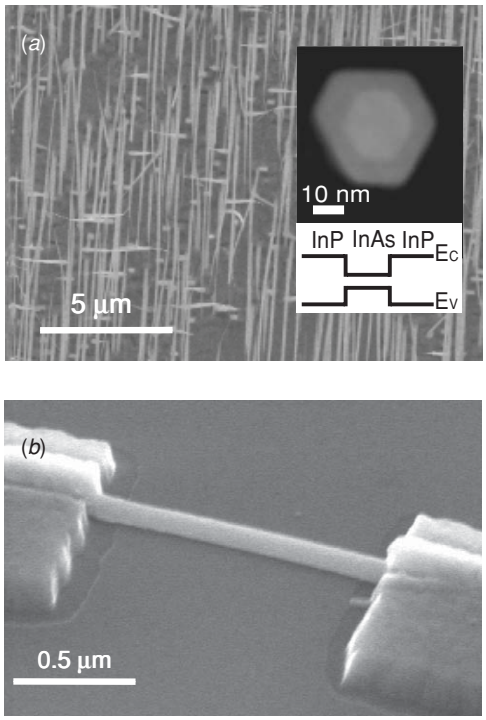

Figure 1. (*a*) Scanning electron microscope (SEM) image of InAs/InP core/shell nanowires grown on an InP substrate. Inset shows a high-angle annular diffraction (HAADF) TEM image of a representative InAs/InP core/shell nanowire. The wire diameter is roughly 20 nm and the shell thickness 7–10 nm. The schematic shows the bandgap alignment for InAs sandwiched between InP. (*b*) SEM image of a typical nanowire device with Ti/Al contacts as used in our measurements.

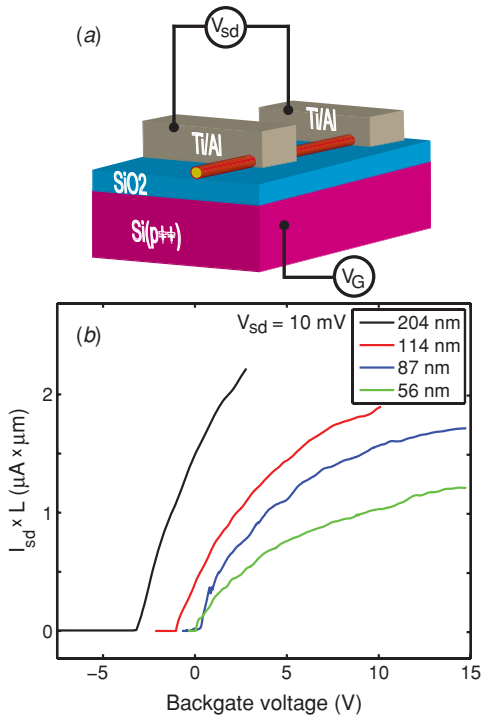

Figure 2. (*a*) Schematic of a Ti/Al contacted nanowire on a heavily doped Si substrate with thermally grown SiO_2 dielectric. (*b*) Current through the nanowire as a function of backgate voltage for several NW diameters.

pointed out that the shell may exhibit a gradual transition from InAsP to InP due to arsenic and phosphorus intermixing at the InAs/InP interface during the InP shell growth [8]. The InAs crystal facets continue through the InP shell, as can be seen in figure 1(*a*), indicating that the InP growth is epitaxial.

The wires are mechanically transferred to a degenerately p-doped Si chip covered with 285 nm SiO_2. The doped Si serves as a gate to control the conduction through the nanowires, see figure 2(*a*). Source-drain contacts to individual nanowires are made via e-beam lithography and e-beam evaporation of Ti/Al (10 nm, 150 nm, respectively). Just before the metal evaporation the sample is dipped into a buffered HF solution for 15 s to remove the native oxides present on the nanowire surface in the areas where contacts will be made, see figure 1(*b*). Typical contacted wire lengths are 1.5–3 μm. Unintentionally doped wires both with and without the InP shell have been measured and show n-type conduction, which can be attributed to the large number of electrons originating from the ionized surface states.

The transport data presented in this work have been taken in vacuum at a temperature of 2K. All nanowires that were contacted did conduct; however, sometimes a positive gate voltage was needed to get ohmic conductance. Applying a negative voltage ($V_G < 0$) to the gate pinches off the conductance through the nanowire as can be seen in figure 2(*b*) for several wires with different diameters. The threshold voltages at which the nanowires pinch off are roughly similar, but typically become more positive for smaller diameters.

From the backgate dependence of the nanowire conductance we calculate the field-effect mobility

$$\mu = g \frac{l^2}{C_{\rm ox}} \frac{1}{V_{\rm SD}} \tag{1}$$

with the NW length l and the transconductance

$$g = \frac{{\rm d}I_{\rm SD}}{{\rm d}V_G}, \tag{2}$$

for constant source-drain bias ($V_{\rm SD}$). V_G is the gate voltage.

MOSFET characterization often uses the effective mobility which gives better fits to the measured conductance [31]. This mobility can be derived from the conductance through the structure at constant gate voltage

$$g_d = \frac{{\rm d}I_{\rm SD}}{{\rm d}V_{\rm SD}}. \tag{3}$$

The expression for the effective mobility then becomes

$$\mu_{\rm eff} = g_d \frac{L^2}{C_{\rm ox}} \frac{1}{V_G - V_{\rm th}}, \tag{4}$$

with $V_{\rm th}$ the threshold voltage. In the field-effect mobility the gate electric field dependence on the mobility is neglected; this will underestimate the true electron mobility, especially at voltages much larger than the threshold voltage. However, for the nanowires studied here, we are mostly interested in the high mobility region close to the threshold voltage. For these voltages the calculated effective mobility strongly depends on the value and definition of the threshold voltage as it goes in

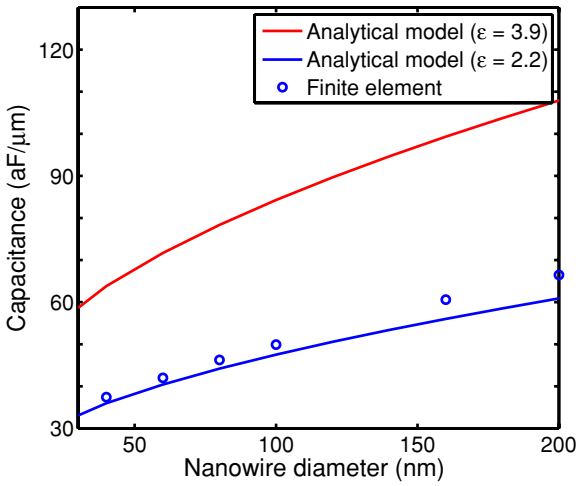

Figure 3. Nanowire capacitance versus diameter using different techniques. Lines represent the calculated capacitances using (5) with $\epsilon = 3.9$ and $\epsilon = 2.2$, respectively. The latter value corresponds to a best fit to finite element calculations [27]. The circles give the nanowire capacitance as obtained from finite element calculations.

the denominator in (4). For this reason we will focus on the field-effect mobility instead. In general the effective mobility gives larger values than the field-effect mobility. Therefore, the numbers obtained in this work should be seen as an lower bound for the true electron mobility.

The difficulty in determining the mobility is in the accurate determination of the gate to nanowire capacitance C_{ox}. We have solved the Poisson equation in a finite element model for several nanowire diameters and compared this to the commonly used model of a metallic cylinder with length l on an infinite conductive plane:

$$C_{ox} = \frac{2\pi\epsilon_{eff}\epsilon_0 l}{\cosh^{-1}[(r + t_{ox})/r]}, \qquad (5)$$

with ϵ_0 the vacuum dielectric constant, r the nanowire radius and t_{ox} the SiO_2 thickness. Since the nanowires are lying on top of the dielectric and are not surrounded by it, instead of using $\epsilon = 3.9$ for SiO_2, we use an effective dielectric constant of $\epsilon_{eff} = 2.2$ as obtained from the best fit from a finite element calculation by Wunnicke [27]. The results of the simulations and the analytical model are depicted in figure 3.

For a small nanowire radius the numbers obtained via (5) using the lowered dielectric constant for SiO_2 compare well to the values obtained using the finite element model. For larger diameters the analytical model underestimates the capacitance [27]. Since the InP shell is very thin we can ignore its contribution to the capacitance.

The gate dependence of the current and the corresponding extracted field effect and effective mobilities are plotted in figures 4(*a*) and (*b*), respectively. Starting from complete pinch-off the nanowire mobility shows a sharp increase just after the onset of conductance and then decays for larger gate voltages and electron densities. This typical decrease in mobility for larger gate voltages has also been observed in InAs wires without a shell. Here it has been attributed to an increased surface scattering and contact Schottky barrier formation to higher sub-bands, effectively

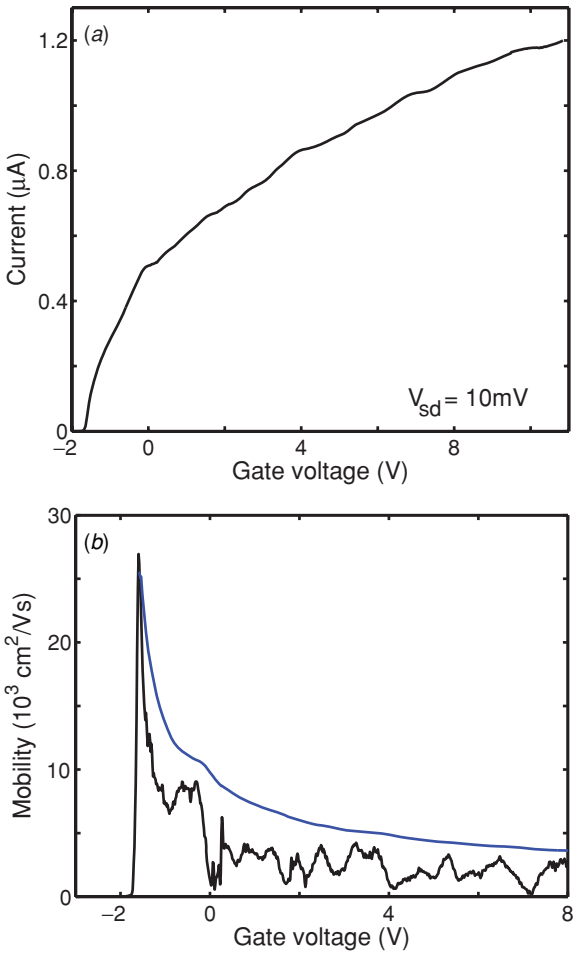

Figure 4. (*a*) Pinch-off curve and (*b*) extracted field effect and effective mobilities for a high mobility core/shell nanowire.

lowering the transconductance of the nanowires [21]. Also an increased wavefunction overlap with the ionized impurities at the surface/interface or increased inter-subband scattering may play a role. Because of possible InAsP formation at the InAs–InP interface, alloy scattering could also limit the mobility for larger gate voltages. The extracted effective mobilities are higher than the field-effect mobilities. Close to the threshold voltage both calculations show similar values; however, in this region the effective mobility is very sensitive to the definition of threshold voltage. The peak field-effect mobility that can be extracted from figure 4 is roughly 25 000 cm^2 V s^{-1}. This is the highest mobility reported so far for surface-treated or core/shell InAs nanowires.

For a large number of nanowires the peak values of the field-effect mobilities are plotted versus the diameter as evaluated from SEM images. Since the wires are tapered, the diameter that has been used is an average for the contacted section. The typical variation in diameter for a 2 μm long nanowire section is around 15 nm. The peak field-effect mobilities versus nanowire diameter are displayed in figure 5(*a*). Mobilities are typically around 10 000 cm^2 V s^{-1} with a large spread around the average. The average is roughly constant versus diameter; however, a slight increase can be observed for smaller diameters. This is contrary to the

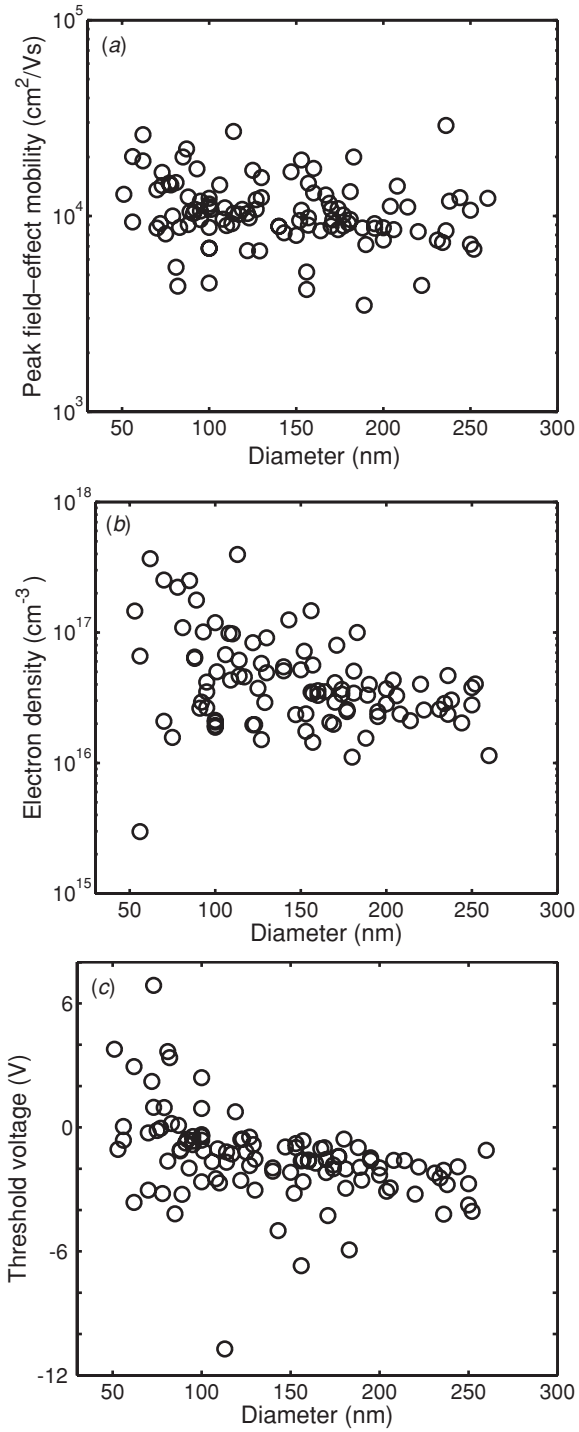

Figure 5. Extracted field effect mobility (*a*), electron density (*b*) and threshold voltage (*c*) versus diameter for a large number of core/shell nanowires.

earlier observation of a drop in mobility for smaller InAs NW diameters. Here, the decrease has been attributed to enhanced surface roughness scattering due to the increased proximity of conduction electrons to the surface [16, 21]. From the almost constant mobilities versus decreasing diameter we conclude that electron backscattering is not affected by the nanowire diameter. This can be either because the surface roughness scattering is no longer the limiting scattering mechanism or because the increased sub-band spacing for small diameters does not increase electron backscattering, despite the increased surface-to-bulk ratio. The spread in the mobility values could be explained by a variation in shell thickness; however, other differences between wires such as the amount of incorporated impurities or crystal twin planes can also play a role.

In figure 5(*c*) we plot the different threshold voltages obtained for different nanowire diameters. For smaller diameter nanowires a more positive voltage has to be applied in order to get conduction. In contrast to what has been claimed by Jiang *et al* [9], we believe that the positive threshold voltages that are needed for small diameter wires are not necessarily indicative of a low amount of impurity doping in the wires. The cross-section decreases with the radius squared and therefore conduction is strongly suppressed for small diameters. A positive gate voltage is needed to get conduction, which explains the positive threshold voltages. This is further supported by our observation of an increase in electron density for reduced nanowire diameters as plotted in figure 5(*b*). The electron density has been calculated from the threshold voltage taking into account the capacitance of the nanowire from (5). The values obtained in that way correspond very well to the electron density as evaluated from the conductance G and mobility without applying a gate voltage ($V_G = 0$):

$$n = \frac{G}{\mu}\frac{l}{eA}, \tag{6}$$

with A the nanowire cross-sectional area.

The increase in electron density in our InAs/InP nanowires for reduced material dimensions is consistent with the observations in bulk InAs [14], in InAs and InN [16, 17] nanowires. For homogeneous conduction through the nanowire, the electron density should be independent of diameter. The increase suggests a radial dependence of electron density with a higher density close to the surface/interface, indicative of a surface or interface accumulation layer. In order to further investigate this dependence we have done measurements on different sections in the nanowires as shown in figure 6(*a*). Since the nanowires are tapered, this allows us to evaluate the electron density for different diameters, while the other nanowire parameters are identical. We clearly see a higher electron density for the smaller diameter sections. Since the InP surface is not known to have a surface accumulation layer, we think that in our case an accumulation layer is formed at the InAs/InP interface [14, 32] as depicted in figure 7(*b*). We have also measured the field-effect mobilities for these sections (not shown); however, they do not demonstrate a dependence versus diameter. This supports the idea that local variations in the amount of incorporated impurities in the nanowire or the number of crystal twin planes have a strong influence on the mobility.

Overall the electron densities for our InAs/InP nanowires are more than an order of magnitude smaller than those obtained for InAs nanowires without a shell, typically 10^{17}–10^{18} cm^{-3} [16, 22, 33, 34]. From figures 5 and 6 we can also see that the change in electron density versus diameter, roughly $2 - 8 \times 10^{14}$ cm^{-3} nm^{-1}, is much smaller than in previously reported bare InAs data, $\sim 2 \times 10^{16}$ cm^{-3} nm^{-1}

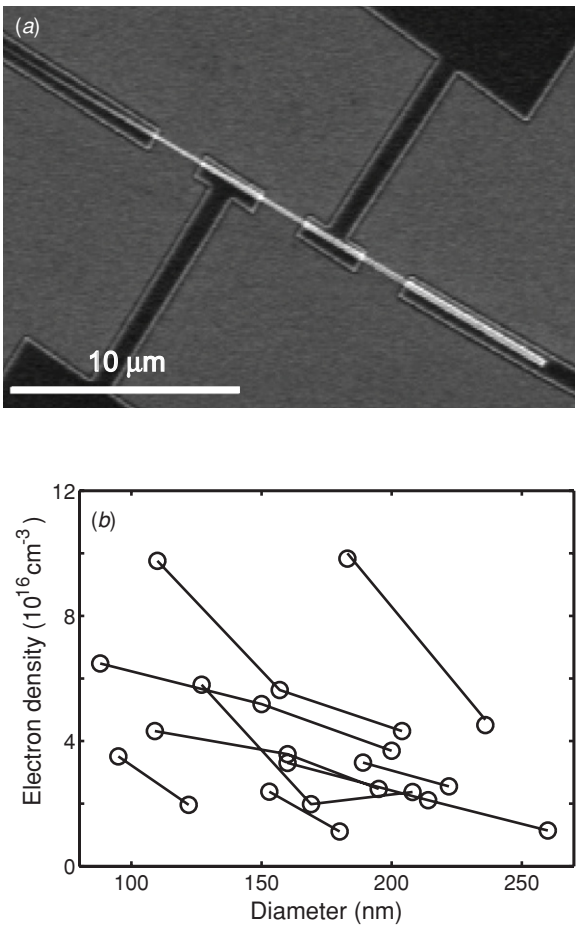

Figure 6. (*a*) SEM image of a nanowire with three contacted sections. Due to tapering the nanowire diameter is different in the two sections which allows extraction of the dependence of electron density on the diameter. (*b*) Electron density versus diameter for different sections inside a single nanowire. The points connected by lines correspond to data extracted from the same nanowire.

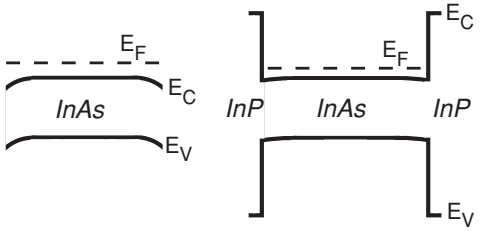

Figure 7. (*a*) Schematic of the bandgap bending of an InAs nanowire and an InAs/InP core/shell nanowire (*b*). Note that the surface band bending is much reduced for the latter case.

[16]. All this points to the conclusion that the accumulation channel at the surface/interface of InAs is reduced in depth and the conduction through the nanowires has a larger relative contribution from electrons in the inner parts of the wire (see figure 7).

In summary, we have grown InP capped InAs nanowires with average low-temperature field-effect mobilities around 10 000 cm^2 V s^{-1} and some exceeding 20 000 cm^2 V s^{-1}. We believe that the increase of field-effect mobility in our system is due to the reduced contribution of electrons from the accumulation layer to the nanowire conduction and a reduced ionized impurity and surface roughness scattering. The nanowire mobilities are roughly constant versus diameter, and do not drop for reduced nanowire dimensions. From this we conclude that electron backscattering is not influenced by the nanowire diameter. A possible explanation would be that the increased surface scattering for reduced nanowire dimensions does not lead to enhanced backscattering because of the larger sub-band spacing. We see a clear indication of an accumulation channel at the interface between InAs and InP; however, from the electron density in the wires we conclude that the depth of the accumulation layer is smaller than the surface accumulation layer that has been observed in InAs nanowires without any capping. From this we conclude that by growing an epitaxial InP shell around InAs nanowires the electron conduction has been changed from mostly shell-like to bulk-like.

Acknowledgments

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