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# Growth and optical properties of axial hybrid III-V/silicon nanowires

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Hybrid silicon nanowires with an integrated light-emitting segment can significantly advance nanoelectronics and nanophotonics. They would combine transport and optical characteristics in a nanoscale device, which can operate in the fundamental single-electron and single-photon regime. III-V materials, such as direct bandgap gallium arsenide, are excellent candidates for such optical segments. However, interfacing them with silicon during crystal growth is a major challenge, because of the lattice mismatch, different expansion coefficients and the formation of antiphase boundaries. Here we demonstrate a silicon nanowire with an integrated gallium-arsenide segment. We precisely control the catalyst composition and surface chemistry to obtain dislocation-free interfaces. The integration of gallium arsenide of high optical quality with silicon is enabled by short gallium phosphide buffers. We anticipate that such hybrid silicon/III-V nanowires open practical routes for quantum information devices, where for instance electronic and photonic quantum bits are manipulated in a III-V segment and stored in a silicon section.

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Silicon has a high thermal conductivity, is mechanically robust and has a stable oxide. Its isotope  $^{28}\text{Si}$  has zero nuclear spin, which makes it especially attractive for quantum information devices<sup>1</sup>, where a single-electron spin is used as a quantum bit<sup>2</sup>. However, Si has an indirect bandgap, significantly limiting photonic applications. In contrast, most III–V's have a direct bandgap and therefore are perfectly suited for optoelectronic devices. Some, such as indium antimonide, also feature a high mobility for electrons and a very strong spin–orbit interaction, the ingredients for nanowire spin–orbit quantum bits (qubits)<sup>3,4</sup>. Importantly, their electronic properties can be tuned by making more complex mixtures, for example ternary or even quaternary compounds. For a wide variety of applications it is valuable to combine the best properties of Si and III–V semiconductors<sup>5–8</sup>, but only if high quality heterojunctions can be realized. In bulk systems, threading dislocations are usually formed at the junction due to a mismatch in lattice constants and thermal expansion coefficients, even for a small lattice mismatch material combination such as GaP/Si (0.3%)<sup>9</sup>. These problems can be solved using bottom–up nanowires grown by the vapour–liquid–solid (VLS) mechanism, in which lattice strain is elastically relieved at the nearby surface<sup>10,11</sup>. Successful examples of high quality interfaces between heavily mismatched materials exist when both materials are from the same semiconductor group<sup>12–14</sup>. But defect-free interfaces between III–V and Si so far remain a challenge, even in nanowires<sup>15</sup>.

In this work, we develop a method to integrate a gallium arsenide section in a silicon nanowire with atomically sharp interfaces, and free of dislocations. Nanowires are grown via the VLS mechanism (see Methods Section) using gold particles. The gold particles catalyse the decomposition of the precursor molecules from the gas phase<sup>16</sup>, and then absorb the elements, forming a liquid alloy. When supersaturation is reached, atoms are expelled to form a crystal (either III–V or Si) below the liquid droplet. We aim at combining different classes of semiconductors, which are normally grown from their corresponding Au-based alloys, such as Au–Ga or Au–Si. To successfully grow III–V/Si heterostructured nanowires, the key is to control the surface chemistry and composition of the alloy. We optimize the growth parameters and in particular for the switching between Si and the III–V semiconductor, which is a critical step. To switch from GaP to Si, a growth interrupt, during which phosphine is removed from the chamber, is essential, as phosphine hinders the absorption of Si in the catalyst particle. For switching from Si to GaP it is important to decrease the growth temperature, and increase the Ga pressure in the gas phase to expel Si from the catalyst alloy. Finally, an optically active GaAs segment is incorporated in the Si wire with good optical quality, as determined from photoluminescence measurements.

## Results

**Optimization of the GaP–Si junction.** First, to initiate uniform nanowire growth, GaP stems are grown at 540 °C on GaP(111) substrates from arrays of gold islands, and after a growth interrupt of several seconds, Si segments are grown on top. Figure 1a shows a scanning electron microscopy (SEM) image of an array of 60 nm-diameter GaP–Si nanowires. We observe that most (95%) of the Si segments grow straight on top of GaP. Importantly, without the growth interrupt, realized by stopping the phosphine supply, we obtain kinked and defected Si segments on GaP as shown in Fig. 1b. The formation of kinked wires has previously been explained by island growth induced by the (solid–solid) hetero-interface energy<sup>15</sup>. In contrast, our results show that phosphine, or one of the decomposition products, kinetically hinders the absorption of Si in the Au particle (at the vapour–liquid

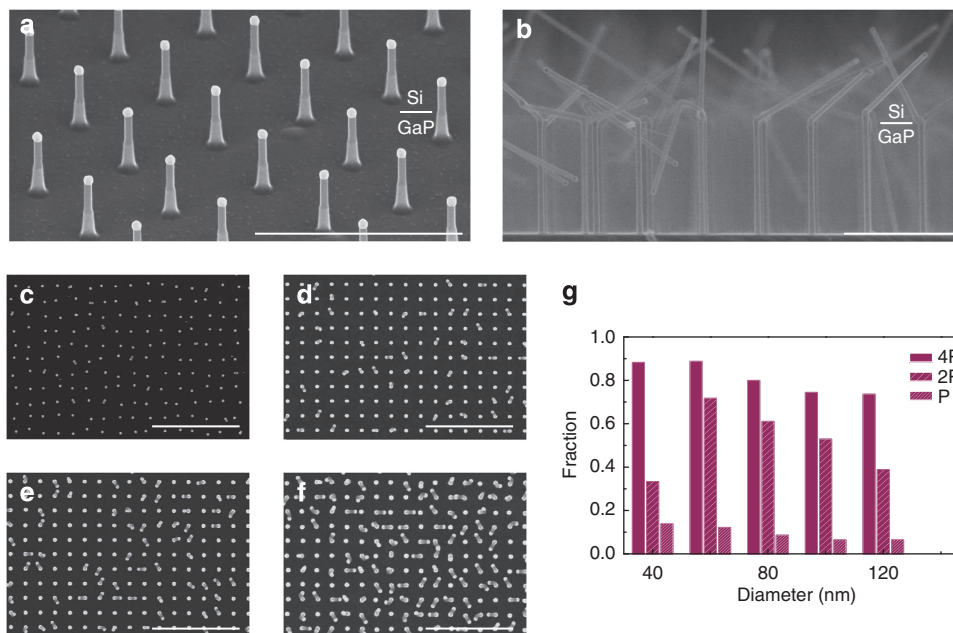
interface), and reduces the supersaturation in the catalyst particle. After the growth interrupt the phosphine is desorbed, and Si atoms can efficiently be absorbed in the droplet. It has been observed before that phosphine affects the nucleation of Si wires<sup>16</sup>, and that at high enough Si supersaturation, proper layer-by-layer growth takes place. As the solubility of group V elements in Au is very low, it is not expected that the solid–liquid interface energy is affected by the growth interrupt.

We statistically analyse kinking at the GaP–Si as a function of wire diameter and disilane pressure. For this study, arrays of Au islands are defined by electron beam lithography with varying particle size and interspacing. From top-view SEM images (Fig. 1c–f), straight and kinked wires are easily recognized as dots and short stripes. The kinking direction is not random, but always along three crystallographic [111] directions. The number of kinked wires increases with the wire diameter. This may either indicate that strain relaxation becomes inefficient or that the filling of the catalyst with silicon is slower for larger particles. The data, summarized in Fig. 1g, also indicate that the number of kinked wires has decreased by a factor of 10 by increasing the disilane pressure by a factor of 4, during the Si nucleation stage. This result shows that a high supersaturation in the catalyst particle is indeed beneficial for the growth of straight Si on GaP.

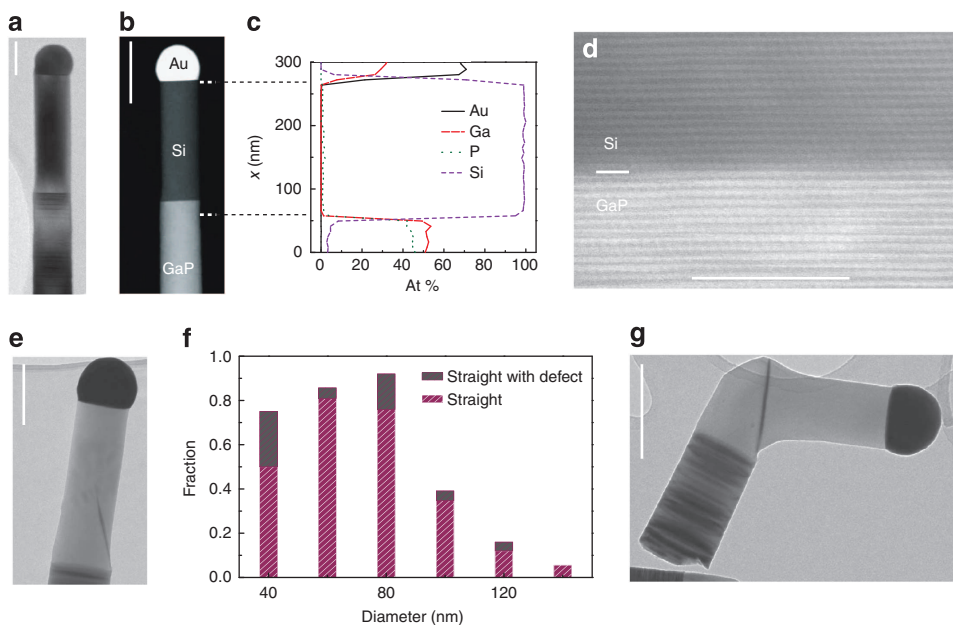
Figure 2a shows a bright-field transmission electron microscopy (TEM) image of a GaP–Si nanowire taken along a  $\langle 110 \rangle$  zone axis. We observe two segments, GaP with stacking faults and Si, which is free of planar defects (see Supplementary Fig. S1 for the image along a different  $\langle 110 \rangle$  zone axis). From the contrast in the dark-field image in Fig. 2b, we distinguish three different materials: the Au nanoparticle on top, the Si segment just below and the GaP segment at the bottom. This stacking is confirmed by energy-dispersive X-ray (EDX) analysis in Fig. 2c. From this EDX scan it is clear that the catalyst particle contains 35% Ga after cooling down, and the Si segment has thus grown from a Au/Ga alloy. We do not observe any effect of the Ga pressure, during the growth of GaP, on the Si growth. The interface between GaP and Si is atomically abrupt, as shown in Fig. 2d, confirming a layer-by-layer growth mechanism of Si on the flat GaP cross-section. We note that a thin Si shell ( $< 2$  nm) forms around the GaP segment during Si growth (Fig. 2c), which is due to the relatively high temperature of the growth process<sup>17</sup>.

TEM measurements reveal that straight wires also can have stacking faults. Typically, for larger diameter wires, we find a set of two inclined twin boundaries in the Si segment (Fig. 2e). These inclined stacking faults are always initiated at the solid–vapour interface of the GaP–Si junction. We present a statistical TEM analysis of these stacking faults in Fig. 2f, and show that for the optimum diameter of 60 nm about 80% of the wires is straight and defect-free. Important to note is that all kinked wires have these inclined stacking faults. A typical example is shown in Fig. 2g. This indicates that the kinked segment has nucleated from the inclined twin plane. With a simple model (see Supplementary Fig. S2), we intuitively explain the formation of the twin planes and the kink. An inclined facet can be formed at the triple-phase point, especially at low supersaturations<sup>18</sup>. Now, nucleation takes place either on the top facet or on the inclined facet. Depending on the contact angles of the catalyst, one of the two nucleation events will dominate. Nucleation on the inclined facet induces a twin and if the catalyst completely moves to the inclined facet a kink is formed.

**Optimization of the Si–GaP junction.** In the next step we aim at fabricating the reversed junction; we grow a GaP segment on Si. The SEM image in Fig. 3a shows an array of uniform GaP–Si–GaP wires. We find an optimum yield (60%) of straight GaP segments grown on Si nanowires at a decreased growth



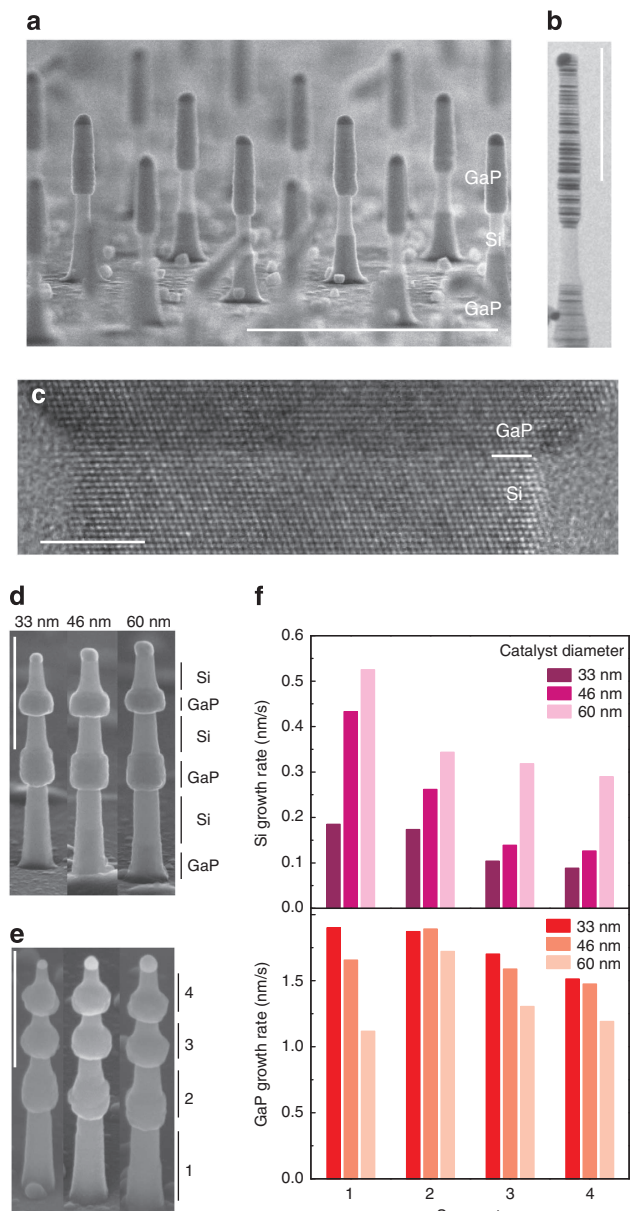
**Figure 1 | GaP-Si nanowire arrays.** (a) SEM image of an array of 60 nm-diameter GaP-Si nanowires with GaP and Si segment lengths of 250 and 300 nm, respectively. Tilt angle = 45°, scale bar, 1 μm. (b) Cross-section SEM image of an array of 60 nm-diameter GaP-Si nanowires with GaP and Si segment lengths of 1 μm and 500 nm, scale bar, 1 μm. (c-f) SEM top-view images of GaP-Si nanowire arrays for different diameters and grown with a Si<sub>2</sub>H<sub>6</sub> partial pressure of 2P = 1.2 × 10<sup>-2</sup> mbar. The pitch is 500 nm for all images, scale bar, 3 μm. The diameters are (c) 40 nm, (d) 70 nm, (e) 100 nm and (f) 120 nm. A dot corresponds to a straight wire. Clearly, the number of kinked wires increases with increasing diameter. (g) Summary of the data for different Si<sub>2</sub>H<sub>6</sub> partial pressures (P = 0.6 × 10<sup>-2</sup> mbar) showing the fraction of straight wires. Each data point is obtained from a field of 625 wires.



**Figure 2 | Structural properties of GaP-Si nanowires.** (a) Bright-field TEM image of a single GaP-Si nanowire, scale bar, 50 nm. (b) High angle annular dark-field (HAADF) image of a single GaP-Si nanowire, scale bar, 100 nm. (c) EDX line scan taken along the nanowire shown in b. (d) High-resolution scanning TEM—HAADF image of the interface between GaP and Si, showing the atomically abrupt interface, scale bar, 5 nm. (e) Bright-field TEM of a straight but faulted GaP-Si nanowire. The twin is clearly visible, scale bar, 100 nm. (f) Plot of the number of straight versus faulted wires observed by TEM. (g) Bright-field TEM of a kinked GP-Si nanowire with visible twins, scale bar, 200 nm.

temperature (500 °C) and increased trimethylgallium partial pressure with respect to the growth of the bottom GaP segment. By decreasing the growth temperature from 540 to 500 °C under H<sub>2</sub> we observe an increase in the yield of straight GaP segments

on Si. We attribute the improved yield to the reduction of the Si concentration in the droplet. Moreover, an excess of Ga is needed in the Au particle to initiate GaP nucleation<sup>19</sup>. From the TEM images (see Fig. 3b,c) it is clear that the GaP segment grows



**Figure 3 | From GaP-Si-GaP multijunctions to superlattice nanowires.**

(a) SEM image of an array of 60 nm-diameter GaP-Si-GaP nanowires with GaP, Si and GaP segment lengths of 180, 150 and 270 nm, respectively. Tilt angle = 80°, scale bar, 1 μm. (b) TEM image of a single GaP-Si-GaP nanowire with a diameter of 28 nm, scale bar, 200 nm. (c) High-resolution TEM picture of a Si-GaP transition, scale bar, 5 nm. Assembled SEM images of (d) triple GaP-Si heterostructures (tilt angle = 80°) with diameters of 33, 46 and 60 nm (left to right), and (e) quadruple GaP-Si heterostructures (tilt angle = 45°) with same diameters, scale bars, 500 nm. (f) Growth rates of GaP and Si segments for nanowires with the various catalyst particle diameters and with respect to their position along the heterostructures in e.

epitaxially on Si. Moreover, the interface between the Si and the GaP segment is atomically abrupt. Under these growth conditions, GaP grows with the zincblende crystal structure and contains stacking faults perpendicular to the growth direction. We also observe a 45% increase in the diameter of the GaP segment compared with that of Si, which is partly explained by an increased particle volume (by the uptake of Ga), and by sidewall

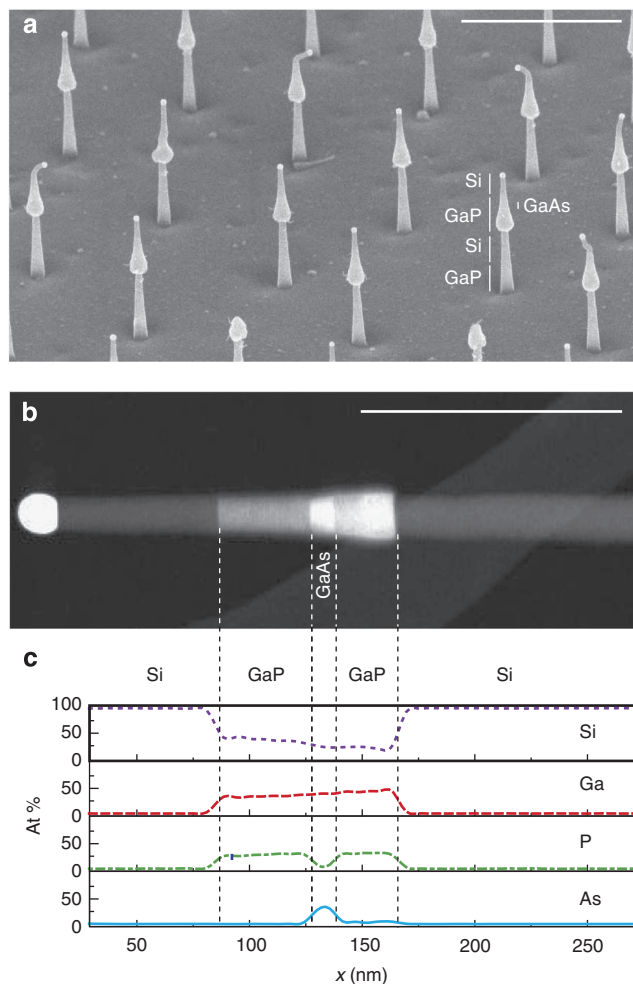
growth at these higher temperatures<sup>20</sup>. However, the most important contribution to the diameter increase comes from differences in contact angle between the Au/Ga alloy on a GaP and on a Si surface. This difference is due to the different surface energies at the solid-vapour, solid-liquid and liquid-vapour interfaces for the Au/Ga-GaP and the Au/Ga-Si systems<sup>21</sup>.

**III-V/Si superlattice nanowires.** The possibility of stacking Si on GaP, and reverse, makes it possible to grow III-V/Si superlattice nanowires. Figure 3d,e show examples of triple and quadruple GaP-Si heterostructures. The heterostructures are straight and show the typical modulation in diameter that is observed when switching from GaP to Si and reverse. An arbitrarily switching scheme is used here and we note that the segment lengths can be optimized on demand for electronic, photonic or phononic applications.

Such applications require materials with specific dimensions, which are controlled by the growth rate. Therefore, the Si and GaP growth rates are studied as a function of the gold catalyst diameter and the position in the vertical direction along the nanowire (Fig. 3f). The growth rates of the upper segments are lower than those of the bottom segments, showing that precursor diffusion along the nanowire facets is rate limiting. The growth rate of the GaP wires is higher for smaller diameters, which is consistent with a constant collection area per wire<sup>22,23</sup>. In contrast to GaP, the Si growth rate increases with the catalyst diameter<sup>24–26</sup>. Two independent factors explain this behaviour: synergetic nanowire growth<sup>27</sup> and the Gibbs-Thomson effect<sup>28,29</sup>. We observe an increase (>15%) of the Si growth rate with decreasing wire-to-wire distance for a constant diameter, which we attribute to synergetic nanowire growth (see Supplementary Fig. S3). The synergetic effect is only relevant for Si interdistances below 1 μm. As the results shown in Fig. 3f are obtained at a larger interdistance (2 μm), this effect can be ignored. A more important contribution comes from the Gibbs-Thomson effect known for increasing the silicon partial pressure in the catalyst upon decreasing the diameter. As a consequence, the incorporation of atoms from the gas phase into the catalyst is reduced<sup>24,25</sup>. We note that the silicon supersaturation inside the catalyst does not only depend on the catalyst radius, but also on the liquid-vapour surface energy. In our case, the silicon precursors do not alloy with pure Au, but with a Au/Ga (65/35) mixture (Fig. 2c). Au/Ga droplets have a much higher (>factor 3) surface energy<sup>21</sup>, shifting the critical diameter, below which no nanowire growth will occur, to higher values. We find a critical diameter of 12 nm (see Supplementary Fig. S4 and Supplementary Table S1). This is four times larger than the value found for Si<sup>24</sup> and Ge<sup>28</sup> nanowires, which is consistent with the higher liquid-vapour interface energy. Generally, it shows that the Gibbs-Thomson effect and the growth dynamics can be tailored by the catalyst chemical composition and surface energy.

**Si wires with an optically active GaAs segment.** We now focus on the incorporation of direct bandgap GaAs into Si nanowires using GaP barriers. The yield of straight Si-GaP-GaAs-GaP-Si (hybrid Si/GaAs) nanowires exceeds 50% (Fig. 4a). The short GaAs segment is visible in the middle of the dark-field image in Fig. 4b and measures 20 nm in length. The complex materials stack is confirmed by the EDX scan along the wire in Fig. 4c. Important to mention is that the GaAs segment is capped with thin GaP and Si shells with thicknesses of 3 and 6 nm, respectively, as calculated from the EDX line scans. The GaAs segment has crystallized in the zincblende crystal structure, containing twin planes and wurtzite sections<sup>20</sup> (see TEM images in Supplementary Fig. S5).



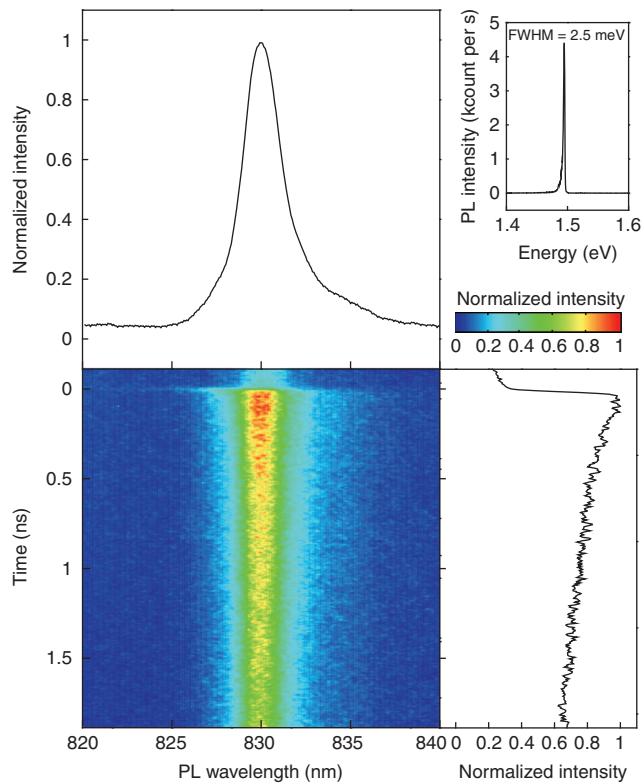


**Figure 4 | GaAs segments in Si nanowires.** (a) SEM picture of an array of GaP-Si-GaP-GaAs-GaP-Si (hybrid Si/GaAs) nanowires. Tilt angle =  $45^\circ$ , scale bar, 1  $\mu\text{m}$ . (b) High angle annular dark-field (HAADF) image of a 25 nm-diameter Si-GaP-GaAs-GaP-Si nanowire, scale bar, 200 nm. (c) EDX scan taken along the nanowire growth axis in b.

We assess the optical quality of our hybrid Si/GaAs nanowires by time-resolved photoluminescence spectroscopy as presented in Fig. 5. The emission from a single GaAs section, with a length exceeding 1  $\mu\text{m}$ , results in a bright and spectrally narrow peak at 1.495 eV (829.5 nm) with full-width half maximum of 2.5 meV (see inset). The 25 meV redshift of the photoluminescence peak, as compared with bulk GaAs can be attributed either to carbon acceptor recombination<sup>29</sup> or to carrier confinement at the interfaces between zincblende and wurtzite crystal phases of GaAs<sup>30</sup>. We determine a lifetime of 7 ns, which is longer than usual exciton lifetimes in pure zincblende GaAs nanowires. This long lifetime originates from indirect recombination of electrons and holes, which are spatially separated at wurtzite/zincblende junctions in the GaAs segment<sup>31</sup>. These long lifetimes lead to an important conclusion—a high purity of the GaAs section. Defects or surface states in a nanowire that typically contribute to very fast nonradiative decay channels are negligible in our hybrid Si/GaAs nanowires.

## Discussion

We have demonstrated epitaxial integration of III-V materials and Si in nanowires. We believe that our approach is generic and



**Figure 5 | Time-resolved photoluminescence spectroscopy of a single hybrid Si/GaAs nanowire measured at 4.2 K.** Colour-coded photoluminescence intensity is plotted as a function of the emission wavelength and detection time after excitation by a laser pulse impinging at time 0. The data at negative times represent the part of the photoluminescence decay that was excited by the previous laser pulse 13 ns earlier. The upper part represents the photoluminescence intensity integrated over the full time window of 2 ns. The right part represents the decay of the photoluminescence spectrum integrated between 825 and 835 nm. The lifetime was determined by extracting the slope of the extrapolated photoluminescence decay curve. Inset: photoluminescence of the same nanowire detected by a nitrogen-cooled silicon array detector. FWHM, full-width half maximum.

allows combining a broad range of semiconductors in an arbitrary sequence, opening new possibilities for device applications. For example, the detection of single photons in the infrared range could be enhanced by the introduction of a low bandgap III-V semiconductor such as GaSb or InAs in the absorption region of Si avalanche nanowire photodiodes<sup>32</sup>. These nanowires have great promise in the field of quantum information processing, for instance spin-orbit quantum bits have recently been shown in III-V wires<sup>3</sup>. However, the electron spin coherence time in this system is relatively short because of interaction with the nuclear spins. A solution could be to integrate a  $^{28}\text{Si}$  segment in a III-V wire as a spin qubit memory element, combining fast qubit operation in III-V<sup>3</sup> and the long coherence time of the spin states in Si<sup>1</sup>.

## Methods

**Patterns.** Regular patterns of gold nanoparticles are prepared by electron beam lithography (100 keV). We define particle diameters ranging from 10 to 250 nm. For each diameter, arrays of  $25 \times 25$  holes are designed with pitches ranging from 200 nm to 5  $\mu\text{m}$ . The GaP(111)B substrate is prepared before resist deposition by etching the surface in a solution of  $\text{HCl}:\text{HNO}_3:\text{H}_2\text{O}$  (3:2:2) at  $50^\circ\text{C}$  for 2 minutes. The resist, a commercial solution of polymethyl methacrylate with 950-k molecular weight, is spin-coated and baked at  $175^\circ\text{C}$  for 15 min. After writing the patterns,

we develop the polymethyl methacrylate in a solution of methyl isobutyl ketone:isopropanol (1:3). A thin layer of 6 nm of gold is evaporated in a vacuum chamber of an electron beam evaporator at a base pressure of  $10^{-8}$  Torr. We realize the liftoff at 70 °C in a commercial solution of PSR3000 for 15 min. Finally, two baths of acetone and one of isopropyl alcohol are required to remove the remaining traces of resist.

**Nanowire growth.** The nanowires are grown in a horizontal Aixtron 200 MOVPE reactor with a total pressure of 25 mbar by the VLS growth mechanism using Au particles, as described above. Before entering the reactor, the samples are chemically treated using a piranha solution. Before growth, we realize annealing at high temperature for decontamination purposes. The growth temperature for GaP–Si and GaP–Si–GaP nanowires is set between 480–610 °C. Above 540 °C, a thin Si shell is formed due to competition between VLS and surface growths. GaAs insertions are grown at temperatures in the range of 450–540 °C. The precursor flow rates are set to  $2 \times 10^{-4}$ – $2 \times 10^{-3}$  mbar for trimethylgallium and  $2 \times 10^{-2}$ – $10 \times 10^{-2}$  mbar for phosphine (PH<sub>3</sub>). The growth interrupt, which consists of removing the PH<sub>3</sub> flow before Si growth, is optimized at 3 s. While growing GaAs segments, the AsH<sub>3</sub> flow is  $8 \times 10^{-3}$  mbar. We studied the influence of P, the Si<sub>2</sub>H<sub>6</sub> partial pressure, at P, 2P and 4P with  $P = 6 \times 10^{-3}$  mbar.

**Micro-photoluminescence.** Micro-photoluminescence studies are performed at 4.2 K. We excite the nanowires with 780 nm picosecond pulsed lasers focused to a spot size of 1 μm using a microscope objective with numerical aperture 0.85. We use an excitation power of 200 nW. We collect the photoluminescence signal by the same objective and send it to a spectrometer, which disperses the photoluminescence onto a nitrogen-cooled silicon array detector or streak camera, enabling 30 μeV spectral and 20 ps temporal resolution, respectively.

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## Author contributions

M.H., M.V., L.K. and E.B. were involved in the design of the experiments. L.K. and E.B. provided guidance throughout the project. M.H. and G.I. were responsible for nanowire growth. M.H. took the lead in the SEM analysis, and M.V. in the TEM analysis. M.H. and N.A. were responsible for the optical measurements. All authors contributed to the writing and editing of the manuscript.

## Additional information

**Supplementary Information** accompanies this paper at <http://www.nature.com/naturecommunications>

**Competing financial interests:** The authors declare no competing financial interests.

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